ELC4438: Embedded System Design

ARM Embedded Processor

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Intro to ARM Embedded Processor

• (UK 1990) Advanced RISC Machines (ARM) Holding

• Produce IP core and license to semiconductor companies
  → produce embedded MPU and MCU according to company strength
  – In electronic design a semiconductor intellectual property core, IP core, or IP block is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party. IP cores may be licensed to another party or can be owned and used by a single party alone.

• Semiconductor companies, e.g. TI, Samsung, Freescale, NXP, ST Semiconductor
ARM Embedded System Support

- Windows CE (Compact/Consumer/Connectivity/Companion – Electronics)
- μClinux (from Linux 2.0/2.4)
- pSOS
- VxWorks (US WindRiver 1983 realtime OS, used in F-16, FA-18, B-2, Patriot SAM, Pathfinder, etc.)
- μC/OS (open source, mostly C coded)
- Palm OS
- Windows 8
ARM Processor Feature

Typical RISC Feature:

• Small volume, low power, low cost, high performance
• Use many registers, fast execution time of instructions
• Easy addressing methods, high-efficiency
• Most data operations done in registers
• 32-bit wordlength
• Embedded online simulator included
ARM Processor Series

- Classic ARM Processors
  - ARM7
  - ARM9
  - ARM11

- Embedded Cortex Processors
  - Cortex-M0
  - Cortex-M1
  - Cortex-M3
  - Cortex-M4
  - Cortex-R4

- Application Cortex Processors
  - Cortex-A5
  - Cortex-A7
  - Cortex-A8
  - Cortex-A9
  - Cortex-A15

(2006)
• ARM [x] [y] [z] [T] [D] [M] [I] [E] [J] [F] [-S]
  – [x] series number ARM7, ARM9
  – [y] memory storage and protection ARM72
  – [z] high-speed buffer ARM720, ARM940
  – [T] Thumb instruction set
  – [D] Support JTAG online/on-chip testing
  – [M] Hardware Multiplier
  – [I] Embedded ICE Macrocell
  – [E] Enhanced DSP instructions
  – [J] Java accelerator Jazelle
  – [F] Floating point
  – [S] Source code, can be applied to EDA (Electronic Design Automation)
Leadership processor technology
- Media acceleration: NEON
- Code density: Thumb
- Security infrastructure: TrustZone

Aligned software development and debug environments
Software compatibility
ARM Cortex

• ARM Cortex-A: Consumer Entertainment Electronics, Wireless Product
  – Cortex-A9/A10 dual-core quad-core 1GHz
  – Cortex-A15 quad-core 2.5GHz

• ARM Cortex-A8  1 GHz
  – Sophisticated pipelining
  – Thumb-2 instruction set (32-bit and 16-bit)
  – NEON™ signal processing – H.264, MP3
  – Jazelle-RCT Java accelerator
  – JIT (Just in Time) and DAC (Dynamic Adaptive Compilation) Technologies
  – e.g. iPad, iPhone4 A4 processor is Cortex-A8 manufactured by Samsung
• The implementation of the Advanced SIMD (Single Instruction, Multiple Data) extension used in ARM processors is called NEON

• SIMD technology uses a single instruction to perform the same operation in parallel on multiple data elements of the same type and size
ARM® Cortex®-A Current Portfolio

Q4 2015

**Cortex-A15**
High-performance with infrastructure feature set

**Cortex-A17**
High-performance with lower power and smaller area relative to Cortex-A15

**Cortex-A57**
Proven high-performance 64/32 bit CPU

**Cortex-A72**
Highest performance 64/32 bit CPU

**Cortex-A9**
Well established mid-range processor used in many markets

**Cortex-A53**
Balanced performance and efficiency 64/32 bit CPU

**Cortex-A5**
Smallest and lowest power, optimized for single-core

**Cortex-A7**
Most efficient ARMv7-A, higher performance than Cortex-A5

**Cortex-A35**
Highest efficiency 64/32 bit CPU

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ARMv7-A

Key: big.LITTLE compatible

ARMv8-A
ARM® Cortex®-R and Cortex-M Processor Portfolio

Q4 2015

Cortex-R4
- Real-time standard

Cortex-R5
- Functional safety

Cortex-R7
- High performance
  - 4G modem and
  - storage

Cortex-M0
- Lowest cost,
  - low power

Cortex-M0+
- Highest energy
  - efficiency

Cortex-M3
- Performance
  - efficiency

Cortex-M4
- Mainstream
  - control & DSP

Cortex-M7
- Maximum
  - performance
  - control & DSP

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ARM Cortex-A8/A9
ARM® Cortex®-A8

- ARM CoreSight™ Debug and Trace
- ARMv7
  32b CPU
- NEON™
  Data Engine
  Floating Point Unit
- 16-32k
  L1 Instruction Cache
- 16-32k
  L1 Data Cache
- Integrated L2 Cache
- 64- or 128-bit AMBA®3 Bus Interface
ACP: Accelerator Coherency Port; SCU: Snoop Control Unit
ARM Cortex-M

- **Cortex-M0**: Lowest cost, Low area
- **Cortex-M0+**: 90 µm, Low power
- **Cortex-M3**: Outstanding energy efficiency, Feature rich connectivity
- **Cortex-M4**: 15 years
- **Cortex-M7**: Digital Signal Control (DSC) processor with DSP, Accelerated SIMD, Floating point (FP)

Scalable and Compatible Architecture

- **Maximum DSC Performance**
- **Flexible Memory System**
- **Cache, TCM, AXI, ECC**
- **Double & Single Precision FP**

Digital Signal Control application space

- ‘8/16-bit’ Traditional application space
- ‘16/32-bit’ Traditional application space
## ARM Cortex-M

<table>
<thead>
<tr>
<th>Cortex-M0</th>
<th>Cortex-M0+</th>
<th>Cortex-M3</th>
<th>Cortex-M4</th>
<th>Cortex-M7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Touchscreen controller</td>
<td>IoT sensor node</td>
<td>Activity trackers and basic wearables</td>
<td>Smart metering and sensor fusion</td>
<td>High-end audio headset or soundbar</td>
</tr>
<tr>
<td>Power management</td>
<td>Bluetooth smart transceiver</td>
<td>Wifi transceiver</td>
<td>High-performance motor control</td>
<td>Automotive (transmission, body electronics, low-cost infotainment)</td>
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</tbody>
</table>
ARM Cortex-M3 Processor

[Diagram of ARM Cortex-M3 Processor with various components like Nested Vectored Interrupt Controller, Wake Up Interrupt Controller Interface, CPU, Code Interface, Memory Protection Unit, SRAM & Peripheral Interface, Bus Matrix, Data Watchpoint, Flash Patch & Breakpoint, Debug Access Port, ITM Trace, ETM Trace, Serial Wire Viewer, Trace Port]
ARM Cortex-M4 Processor

![Diagram of ARM Cortex-M4 Processor]](image)
ARM Cortex-M4 Processor

Energy efficient digital signal control

• The Cortex-M4 processor has been designed with a large variety of highly efficient signal processing features

• The Cortex-M4 processor features extended single-cycle multiply accumulate (MAC) instructions, optimized SIMD arithmetic, saturating arithmetic instructions and an optional single precision Floating Point Unit (FPU).
ARM Cortex-M4 Processor

Responsiveness and low power

• The Cortex-M4 has integrated sleep modes and optional state retention capabilities which enable high performance at a low level of power consumption.

• The processor executes the Thumb-2 instruction set for optimal performance and code size.

• The Cortex-M4 Nested Vectored Interrupt Controller is highly configurable at design time to deliver up to 240 system interrupts with individual priorities, dynamic reprioritization and integrated system clock.
# ARM Cortex-M4 Features

<table>
<thead>
<tr>
<th>ISA Support</th>
<th>Thumb / Thumb-2</th>
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</thead>
</table>
| DSP Extensions    | Single cycle 16/32-bit MAC  
|                   | Single cycle dual 16-bit MAC  
|                   | 8/16-bit SIMD arithmetic  
|                   | Hardware Divide (2-12 Cycles) |
| Floating Point Unit | Single precision floating point unit  
|                   | IEEE 754 compliant |
| Pipeline          | 3-stage + branch speculation |
| Performance Efficiency | Without FPU: 1.25 / 1.52 / 1.91 DMIPS/MHz*  
|                   | With FPU: 1.27 / 1.55 / 1.95 DMIPS/MHz* |

* Dhrystone **MIPS** (Million Instructions per Second), or **DMIPS**, is a measure of computer performance relative to the performance of the DEC VAX 11/780 minicomputer of the 1970s.
## ARM Cortex-M4 Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Memory Protection</strong></td>
<td>Optional 8 region MPU with sub regions and background region</td>
</tr>
<tr>
<td><strong>Interrupts</strong></td>
<td>Non-maskable Interrupt (NMI) + 1 to 240 physical interrupts</td>
</tr>
<tr>
<td><strong>Interrupt Priority Levels</strong></td>
<td>8 to 256 priority levels</td>
</tr>
<tr>
<td><strong>Wake-up Interrupt Controller</strong></td>
<td>Up to 240 Wake-up Interrupts</td>
</tr>
<tr>
<td><strong>Sleep Modes</strong></td>
<td>Integrated WFI and WFE Instructions and Sleep On Exit capability.</td>
</tr>
<tr>
<td></td>
<td>Sleep &amp; Deep Sleep Signals.</td>
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<td></td>
<td>Optional Retention Mode with ARM Power Management Kit</td>
</tr>
<tr>
<td><strong>Bit Manipulation</strong></td>
<td>Integrated Instructions &amp; Bit Banding</td>
</tr>
<tr>
<td><strong>Debug</strong></td>
<td>Optional JTAG &amp; Serial-Wire Debug Ports. Up to 8 Breakpoints and 4 Watchpoints.</td>
</tr>
<tr>
<td><strong>Trace</strong></td>
<td>Optional Instruction Trace (ETM), Data Trace (DWT), and Instrumentation Trace (ITM)</td>
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